Amendments

In the Claims:

Please substitute the following claims 1-9 and 12 for the pending claims 1-9 and 12:

1. (Amended) A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current; and

a write switch including plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

2. (Amended) The one-time programming memory element according to claim 1, wherein said capacitor oxide layer is approximately 20Å thick.

3. (Amended) The one-time programming memory element according to claim 1, wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said switch and a gate dielectric forming said oxide layer.

4. (Amended) The one-time programming memory element according to claim 3, wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions;

a deep N-well layer below the P-well layer; and

a P-type substrate below the deep N-well layer.

5. (Amended) The one-time programming memory element according to claim 1, wherein said write switch comprises a 5 volt tolerant switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage is less than 7 volts.

6. (Amended) The one-time programming memory element according to claim 1, further comprising a sensing circuit to sense whether said capacitor is programmed.

7. (Amended) The one-time programming memory element according to claim 1, wherein a charge pump is not required to program said anti-fuse.

8. (Amended) A process, compatible with 0.13μm or below CMOS technology, for making a one-time programming memory element, comprising the steps of:

forming a capacitor having an oxide layer capable of passing direct gate tunneling current; and

forming a write switch including plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse, without a charge pump, by application of a voltage across said capacitor oxide layer via said switch to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

9. (Amended) The process according to claim 8, wherein said capacitor oxide layer is formed to a thickness of approximately 20Å thick.

12. (Amended) The process according to claim 8, wherein said forming switch step comprises forming a 5 volt tolerance switch having plural 2.5 volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage is less than 7 volts.

Please add the following new claims 15-21:

15. (New) The one-time programming element of claim 1, wherein said plural transistors of said write switch include:

a first switch transistor coupled between a first voltage and a first terminal of said capacitor; and

a second switch transistor coupled between a second voltage and a second terminal of said capacitor, wherein closing said first and second switch transistors causes application of said voltage across said capacitor oxide layer.

16. (New) The one-time programming element of claim 1, further comprising:

a read transistor, coupled to said capacitor, having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer.

17. (New) The one-time programming element of claim 1, wherein said voltage applied across said capacitor oxide layer is less than 7 volts.

18. (New) A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer, approximately 20Å thick, capable of passing direct gate tunneling current; and

a write switch having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said oxide layer via said switch to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

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19. (New) A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current;

and

a write switch having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage across said oxide layer via said switch to rupture said oxide layer to form a conductive path having a resistance of approximately hundreds of ohms or less;

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wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said switch and a gate dielectric forming said oxide layer; and

wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions,

a deep N-well layer below the P-well layer, and

a P-type substrate below the deep N-well layer.

20. (New) A one-time programming memory element capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a transistor configured as a capacitor and having an oxide layer capable of passing direct gate tunneling current;

a write circuit, including:

a first switch transistor connected between a first terminal of said capacitor and a first voltage, and

a second switch transistor connected between a second side of said capacitor opposing said first side and a second voltage; and

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage, equal to a difference between said first and second voltages, across said oxide layer when said first and second switches are closed.

21. (New) The one-time programming memory element of claim 21, wherein each said first and second switch transistor has an oxide layer thicker than said capacitor oxide layer.